

Yu (Kevin) Cao

Assistant Professor, Electrical Engineering
Affiliated Professor, Computer Science and Engineering

Department of Electrical Engineering, Arizona State University
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Education

- 1997 – 2002 University of California, Berkeley, CA, USA
Ph.D. in Engineering – EECS (December 2002)
Dissertation: *Nanometer Circuit Performance Analysis: Device and Interconnect*
Advisor: Professor Chenming Hu
M.A. in Biophysics (December 1999)
- 1991 – 1996 Peking University, Beijing, China
B.S. in Physics (July 1996)

Experience

- 11/04 – Assistant Professor, Department of Electrical Engineering, Arizona State University
- 2003 – 2004 Post-Doctoral Researcher, University of California, Berkeley
Berkeley Wireless Research Center, Advisor: Professor Jan M. Rabaey
- 1999 – 2002 Graduate Student Researcher, University of California, Berkeley
Device Group, Department of EECS, Advisor: Professor Chenming Hu
- 2001 Summer Research Intern, IBM Microelectronics Division, Hopewell Junction, NY
- 2000 Summer Research Intern, Hewlett-Packard Laboratories, Palo Alto, CA

Teaching Experience

- EEE 333: Hardware Design Languages and Programmable Logic (Spring 2008, Fall 2008)
- EEE 425: Digital Systems and Circuits (Fall 2005)
- EEE 525: VLSI Design (Spring 2005, Spring 2006, Spring 2007, Fall 2007)
- EEE 598: Modeling and Design for Nano-CMOS Technology (Developed, Fall 2006)

Honors and Awards

- 2008 Chunhui Award for Outstanding Oversea Chinese Scholars, China
- 2007 Best Paper Award, International Symposium on Low Power Electronics and Design
- 2007 IBM Faculty Award
- 2006 NSF Faculty Early Career Development (CAREER) Award
- 2006 IBM Faculty Award
- 2004 Best Paper Award, International Symposium on Quality Electronic Design

- 2000 Beatrice Winner Award, International Solid-State Circuits Conference
- 1997 Biophysics Graduate Program Fellowship, University of California, Berkeley
- 1996 Regents Fellowship, University of California, Santa Cruz

Research Interests

- Predictive modeling of nanoscale CMOS and post-silicon technologies
- Physical-level design and tools for variability and reliability
- Reliable integration of emerging technologies
- Low-power design solutions

Teaching Interests

- Undergraduate: solid-state devices, digital circuits and systems, VLSI design and synthesis analog integrated circuits, computer architecture
- Graduate: device modeling, VLSI design for nanoscale technology, computer-aided design

Professional Service

- Guest Editor, *IEEE Design & Test of Computers*, Special Issue on Design for Reliability, 2009
- Co-chair, Circuit Reliability Committee, *IEEE International Reliability Physics Symposium (IRPS)*, 2009
- Co-organizer of *IEEE/ACM Workshop on Compact Variability Modeling (CVM)*, 2008
- Chair, Device Modeling and Simulation Subcommittee, *IEEE International Conference on Computer-Aided Design (ICCAD)*, 2008
- Chair, Design Contest, *ACM/IEEE International Symposium on Low Power Electronics Design (ISLPED)*, 2008
- Member of the Compact Modeling Technical Committee, IEEE Electron Devices Society, 2007 – present
- Publicity Chair, IEEE Solid-State Circuits Society, Phoenix Chapter, 2006 – 2007
- Technical Program Committee member:
 - *ACM/IEEE Design Automation Conference (DAC)*, 2007 – 2008
 - *IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, 2006 – 2009
 - *ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, 2005 – 2008
 - *IEEE International Conference on Computer Design (ICCD)*, 2005 – 2007
 - *ACM/IEEE International Symposium on Low Power Electronics Design (ISLPED)*, 2005 – 2008
 - *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2008
 - *ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, 2007
- Session Chair, DAC 2005/2007, ISLPED 2005/2007, ICCAD 2005/2006, ICCD 2005, ISQED 2006
- Book proposal reviewer, Morgan Kaufmann Publishers Inc.
- Reviewer for:
 - *IEEE Transactions on Computer-Aided Design*, *IEEE Transactions on Electron Devices*, *IEEE Journal of Solid-State Circuits*, *IEEE Transactions on VLSI Systems*, *IEEE Electron*

- Device Letters, IEEE Transactions on Circuits and Systems, IEEE Circuits and Devices Magazine, IEEE Transactions on Nanotechnology*
- *ACM Transactions on Design Automation of Electronic Systems, ACM Journal of Emerging Technologies in Computing Systems*
 - *IBM Journal of Research and Development*
 - *IET Proceedings of Circuits, Devices and Systems, IET Electronics Letters*
 - *Elsevier Solid State Electronics*
 - *Journal of Low Power Electronics*
 - *National Science Foundation*
 - *Springer Science+Business Media, LLC*
 - *University of Arizona ADVANCE program*
 - *University of California MICRO program*

University Service

- Solid-State Circuits Master (MSE) graduate advisor, 2005 – present
- Curriculum development of the Solid-State Circuits group at ASU, 2005 – present

Consulting Experience

- Anova Solutions Inc., Santa Clara, CA
- Rio Design Automation Inc., Santa Clara, CA
- Seiko EDA Technologies Inc., Japan
- Celestry Design Technologies Inc., San Jose, CA

Students

Ph.D. Graduate Students

- Min Chen (expected to graduate in May 2009)
- Anupama Subramaniam (part-time, Marvell Technology Group Ltd.)
- Chi-Chao Wang
- Wei Zhao (defense scheduled on November 5th, 2008)
- Yun Ye
- Wenping Wang (June 2008, Thesis “Circuit aging in scaled CMOS design: modeling, simulation, and prediction,” now with Vitesse Semiconductor Corp.)
- Asha Balijepalli (co-advised with Prof. Trevor Thornton, December 2007, Thesis “Compact modeling and applications of a PD SOI MESFET,” now with Advanced Micro Devices, Inc.)

Master Graduate Students

- Varsha Balakrishnan
- Saurabh Sinha
- Dinesh Ganesan (December 2007, Thesis “Finite point gate model,” now with Freescale Semiconductor, Inc.)
- Ritu Singhal (September 2007, Thesis “Compact modeling of non-rectangular gate effect,” now with Microchip Technology, Inc.)
- Rakesh Vattikonda (July 2007, Thesis “Predictive modeling of NBTI effect,” now with Broadcom Corp.)
- Tarun Sairam (July 2006, Thesis “Low-power digital design with FinFET technology,” now with Sun Microsystems, Inc.)

Invited Talks and Presentations

Invited Talks

- Asia and South Pacific Design Automation Conference, Tutorial, “Circuit Reliability: Modeling, Simulation, and Resilient Design Solutions,” Yokohama, Japan, 2009.
- International On-Line Testing Symposium, Invited Talk, “Modeling and Simulation of Circuit Aging in Scaled CMOS Design,” Rhodes, Greece, July 2008.
- International Reliability Physics Symposium, Tutorial, “Reliability Modeling and Simulation for Sub-45nm Design,” Phoenix, AZ, April 2008.
- International Conference on Computer-Aided Design, Embedded Tutorial, “MOSFET modeling for 45nm and beyond,” San Jose, November, 2007.
- Synopsys Engineering Seminar Series (SESS), “Predictive Technology Modeling for Robust Circuit Design with Nano-CMOS and Post-Silicon Technologies,” Sunnyvale, CA, December 2006.
- International Conference on Nano-Networks, Invited Talk, “Predictive Technology Model for Nano-CMOS Design Exploration,” Lausanne, Switzerland, September 2006.
- Synopsys Engineering Seminar Series (SESS), “Coping with Process Uncertainties in Circuit Modeling and Simulation,” Sunnyvale, CA, September 2006.
- Semiconductor Research Corporation (SRC) Technology Transfer e-Workshop, “Benchmarking Nanoscale Circuit Reliability with Predictive Technology Models,” August 2006.
- Intel External Long-range Research Seminar (ELRS), “Predictive Technology Modeling for Reliable Nanoscale Integration,” San Jose, CA, August 2006.

Others

- ARM, “Reliable Integration with Unreliable Nanoscale Devices: Predictive Modeling and Design Solutions,” Sunnyvale, CA, March 2008.
- University of Washington, Department of Electrical Engineering, Research Colloquium, “Predictive Technology Model for Nanoelectronic Design,” Seattle, WA, November 2007.
- Tsinghua University and Southeast University, “Predictive Technology Modeling in the Nanoelectronics Era,” China, May 2007.
- Intel, “Coping with Process Variations in Circuit Modeling and Simulation,” Santa Clara, CA, February, 2007
- IBM, “Predictive Modeling of NBTI Effects for Reliable Nanoscale Design,” Austin, TX, February 2007.
- University of California, Los Angeles, “Bridging Nanometer to Gigascale: Predictive Technology Modeling for Robust IC Design,” November 2006.
- Texas Instruments, “Predictive Modeling of Variability and Reliability in Nanoscale Design,” Dallas, TX, November 2006.
- Qualcomm, “Benchmarking Nanoscale Circuit Design with Predictive Design Model,” San Diego, CA, October 2006.
- Tsinghua University and Peking University, “Bridging Nanometer to Gigascale: Predictive Technology Model for Robust Nanometer Integration,” Beijing, China, May 2006.
- LSI Logic, “Predictive Technology Model for Robust Nanoscale Integration,” Milpitas, CA, March 2006.
- Intel, “Modeling and Simulation of Variability and Reliability Issues for Robust Nanometer Design,” Santa Clara, CA, March 2006.

- Arizona State University, Center for Solid State Electronics Research (CSSER) Seminar, “Predictive Technology Model for Robust Nanoscale Integration,” Tempe, AZ, February 2006.
- IBM T. J. Watson Research Center and Austin Research Laboratories, “Modeling and Simulation of Variability and Reliability Issues for Robust Nanometer Design,” Yorktown Heights, NY and Austin, TX, February 2006.
- Synopsys, “Benchmarking Sub-45nm Circuits Design with Predictive Technology Models,” Sunnyvale, CA, January 2006.
- IBM Austin Research Laboratories, “Variability Modeling and Characterization for Robust Nanometer Design,” Austin, TX, August 2005.
- Synopsys, “Bridging the Technology-EDA Gap: Variability Modeling and Characterization for Robust Nanometer Design,” Sunnyvale, CA, August 2005.
- Intel, “Bridging Nanometer to Gigascale: Process Variation Modeling for Reliable Design,” Santa Clara, CA, February 2005.

Professional Memberships

- Member, Institute of Electrical and Electrical Engineers (IEEE)
- Member, Association for Computing Machinery (ACM)

Patent

- Xia Li, Wei Zhao, David Bang, Yu Cao, Seung H. Kang, Matt Nowak, “A contact and via module of advanced on-chip interconnect technology,” application submitted, 2008.
- Xia Li, Wei Zhao, Yu Cao, Sam Gu, Seung H. Kang, Matt Nowak, “An interconnect module of advanced on-chip interconnect technology,” application submitted, 2008.
- Norman Chang, Yu Cao, Osamu Samuel Nakagawa, Shen Lin, Weize Xie, “System for improving circuit simulations by utilizing a simplified circuit model based on effective capacitance and inductance values,” US patent-6567960, May 20, 2003.

Publications (advisee names in bold; citation numbers from Google Scholar)

Book

B. Wong, A. Mittal, Y. Cao, and G. Starr, *Nano-CMOS Circuit and Physical Design*, John Wiley & Sons, Inc., 2004. [used as the textbook/main reference by **University of California, Berkeley, University of Michigan, and Chang Gung University, Taiwan; under the translation to Chinese**]

Journal Papers (total journal papers with ASU students: 14)

Under Review

- [1] **D. Ganesan**, A. Mitev, **M. Chen**, Y. Cao, J. M. Wang, “Charge-based finite-point gate model for fast timing and power analysis,” submitted to *IEEE Transactions on VLSI Systems*.
- [2] F. Pan, W. Xu, T. Dastagir, **S. Sinha**, Y. Cao, H. Yu, “Improved frequency response of wideband on-chip inductors with patterned magnetic dots,” submitted to *IEEE Electron Device Letters*.
- [3] **A. Balijepalli**, **S. Sinha**, Y. Cao, “Compact model of carbon nanotube transistor and interconnect,” submitted to *IEEE Transactions on Electron Devices*.
- [4] **W. Zhao**, F. Liu, K. Agarwal, D. Acharyya, S. R. Nassif, K. Nowka, Y. Cao, “Rigorous extraction of process variations for 65nm CMOS design,” submitted to *IEEE Transactions on Semiconductor Manufacturing*.

- [5] L. Cheng, Y. Lin, L. He, and Y. Cao, "Trace-based framework for concurrent development of process and FPGA architecture considering process variation and reliability," submitted to *ACM Transactions on Design Automation of Electronic Systems*.
- [6] **R. Singal, A. Balijepalli, A. Subramaniam**, F. Liu, S. Nassif, Y. Cao, "Modeling and analysis of the non-rectangular gate effect for post-lithography circuit simulation," submitted to *IEEE Transactions on VLSI Systems*.
- [7] **W. Wang**, S. Yang, S. Bhardwaj, **R. Vattikonda**, S. Vrudhula, F. Liu, Y. Cao, "A comprehensive analysis of NBTI effect in combinational and sequential circuits," submitted to *IEEE Transactions on VLSI Systems*.

Accepted or Published

- [8] J. M. Wang, Y. Cao, **M. Chen**, J. Sun, A. Mitev, and K. Potluri, "Capturing device mismatch in analog and mixed-signal design," to be published in *IEEE Circuits and Systems Magazine*, 2008. **[invited]**
- [9] **M. Chen, W. Zhao**, F. Liu, Y. Cao, "Finite-point based transistor model: A new approach to fast circuit simulation," to be published in *IEEE Transactions on VLSI Systems*, 2008.
- [10] **A. Balijepalli**, J. Ervin, W. Lepkowski, Y. Cao, and T. Thornton, "Compact modeling of a PD SOI MESFET for wide temperature designs," to be published in *Microelectronics Journal*, Elsevier Ltd., 2008.
- [11] S. Bhardwaj, **W. Wang, R. Vattikonda**, Y. Cao, S. Vrudhula, "A scalable model for predicting the effect of NBTI for reliable design," *IET Circuits, Devices & Systems*, vol. 2, no. 4, pp. 361-371, 2008.
- [12] T. Austin, V. Bertacco, S. Mahlke, Y. Cao, "Reliable systems on unreliable fabrics," *IEEE Design & Test of Computers*, vol. 25, no. 4, pp. 322-332, July/August, 2008. **[invited]**
- [13] B. H. Calhoun, Y. Cao, X. Li, K. Mai, L. T. Pileggi, R. A. Rutenbar, and K. L. Shepard, "Digital circuit design challenges and opportunities in the era of nanoscale CMOS," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 343-365, February 2008. **[invited]**
- [14] **W. Wang**, V. Reddy, A. T. Krishnan, **R. Vattikonda**, S. Krishnan, Y. Cao, "Compact modeling and simulation of circuit reliability for 65nm CMOS technology," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 509-517, December 2007. **[invited]**
- [15] Y. Cao and L. T. Clark, "Mapping statistical process variations toward circuit performance variability: an analytical modeling approach," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 10, pp. 1866-1873, October 2007.
- [16] **W. Zhao** and Y. Cao, "Predictive technology model for nano-CMOS design exploration," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 3, no. 1, pp. 1-17, April 2007.
- [17] H. Qin, **R. Vattikonda**, T. Trinh, Y. Cao, J. Rabaey, "SRAM cell optimization for ultra-low power standby," *ASP Journal of Low Power Electronics*, vol. 2, no. 3, pp. 401-411, December 2006.
- [18] **W. Zhao**, Y. Cao, "New generation of predictive technology model for sub-45nm early design exploration," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2816-2823, November 2006.
- [19] J. He, M. Fang, B. Li, G. Zhang, Y. Cao, "A new analytic approximation to general diode equation," *Solid-State Electronics*, Elsevier Ltd., vol. 50, no. 9, pp. 1371-1374, September 2006.

- [20] S. Bhardwaj, Y. Cao, S. Vrudhula, "Statistical leakage minimization of digital circuits using gate sizing, gate length biasing, and threshold voltage selection," *ASP Journal of Low Power Electronics*, vol. 2, no. 2, pp. 240-250, August 2006.
- [21] J. Chen, L. T. Clark, and Y. Cao, "Maximum Fan-In/Out: Ultra-low voltage circuit design in the presence of variations," *IEEE Circuits and Devices Magazine*, vol. 21, no. 6, pp. 12-20, November 2005.
- [22] Y. Cao, X.-D. Yang, X. Huang, and D. Sylvester, "Switch-factor based loop RLC modeling for efficient timing analysis," *IEEE Transactions on VLSI Systems*, vol. 13, no. 9, pp. 1072-1078, September 2005.
- [23] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu, and J. M. Rabaey, "Standby supply voltage minimization for deep sub-micron SRAM," *Microelectronics Journal*, Elsevier Ltd., vol. 36, no. 9, pp. 789-800, September 2005.
- [24] Y. Cao, X. Huang, D. Sylvester, T.-J. King, and C. Hu, "Impact of on-chip interconnect frequency-dependent $R(f)L(f)$ on digital and RF design," *IEEE Transactions on VLSI Systems*, vol. 13, no. 1, pp. 158-162, January 2005.
- [25] R. Chang, Y. Cao, and C. Spanos, "Modeling metal dishing for interconnect optimization," *IEEE Transactions on Electron Devices*, vol. 51, no. 10, pp. 1577-1583, October 2004.
- [26] Y. Cao, M. Orshansky, D. Sylvester, T. Sato, and C. Hu, "SPICE up your MOSFET modeling: presenting a new paradigm of predictive MOSFET modeling for early circuit design innovation," *IEEE Circuits and Devices Magazine*, vol. 19, no. 4, pp. 17-23, July 2003.
- [27] T. Sato, Y. Cao, K. Agarwal, D. Sylvester, and C. Hu, "Bidirectional closed-form transformation between on-chip coupling noise waveforms and interconnect delay change curves," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 5, pp. 560-572, May 2003.
- [28] Y. Cao, R. A. Groves, N. D. Zamdmer, J. Plouchart, R. A. Wachnik, X. Huang, T. King, and C. Hu, "Frequency-independent equivalent circuit model for on-chip spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 419-426, March 2003. **[cited by 118]**
- [29] X. Huang, P. Restle, T. Bucelot, Y. Cao, and T. King, "Loop-based interconnect modeling and optimization approach for multi-GHz clock network design," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 457-463, March 2003.
- [30] Y. Cao, C. Hu, X. Huang, A. B. Kahng, I. L. Markov, M. Oliver, D. Stroobandt, and D. Sylvester, "Improved a priori interconnect predictions and technology extrapolation in the GTX system," *IEEE Transactions on VLSI Systems*, vol. 11, no. 1, pp. 3-14, February 2003.
- [31] Y. Cao, X. Huang, N. Chang, S. Lin, O. S. Nakagawa, W. Xie, D. Sylvester, and C. Hu, "Effective on-chip inductance modeling for multiple signal lines and application on repeater insertion," *IEEE Transactions on VLSI Systems*, vol. 10, no. 6, pp. 799-805, December 2002.
- [32] T. Sato, D. Sylvester, Y. Cao, and C. Hu, "Accurate in-situ measurement of peak noise and signal delay induced by interconnect coupling," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1587-1591, October 2001.

Conference Papers (total conference papers with ASU students: 33)

- [1] M. Debole, R. Krishnan, **W. Wang, V. Balakrishnan**, H. Luo, Y. Wang, Y. Cao, Y. Xie, V. Narayanan, "New-Age: A framework for NBTI estimation," to be published at *Asia and South Pacific Design Automation Conference*, 2009.

- [2] **W. Wang, V. Balakrishnan, B. Yang**, Y. Cao, “Statistical prediction of NBTI-induced circuit aging,” to be published at *International Conference on Solid-State and Integrated-Circuit Technology*, 2008. [invited]
- [3] M. Agarwal, **V. Balakrishnan**, A. Bhuyan, K. Kim, B. C. Paul, **W. Wang**, Y. Cao, S. Mitra, “Optimized circuit failure prediction for aging: practicality and promise,” to be published at *International Test Conference*, 2008.
- [4] **C.-C. Wang, W. Zhao**, Y. Cao, “Predictive modeling of layout-dependent carrier mobility in stressed CMOS technology,” to be published at *SRC TECHNON*, 2008.
- [5] **V. Balakrishnan, W. Wang**, Y. Cao, “Statistical prediction of circuit aging under process and design uncertainties,” to be published at *SRC TECHNON*, 2008.
- [6] **W. Wang**, V. Reddy, **B. Yang, V. Balakrishnan**, S. Krishnan, Y. Cao, “Statistical prediction of circuit aging under process variations,” *Custom Integrated Circuits Conference*, pp. 13-16, 2008.
- [7] **Y. Ye**, F. Liu, S. Nassif, Y. Cao, “Statistical modeling and simulation of threshold variation under dopant fluctuations and line-edge roughness,” *Design Automation Conference*, pp. 900-905, 2008. [acceptance rate: 20%]
- [8] **S. Sinha, A. Balijepalli**, Y. Cao, “A simplified model of carbon nanotube transistor with applications to analog and digital design,” *International Symposium on Quality Electronic Design*, pp. 502-507, 2008.
- [9] **W. Wang**, S. Yang, and Y. Cao, “Node criticality computation for circuit timing analysis and optimization under NBTI effect,” *International Symposium on Quality Electronic Design*, pp. 763-768, 2008.
- [10] X. Li, Y. Cao, “Projection-based piecewise-linear response surface modeling for strongly nonlinear VLSI performance variations,” *International Symposium on Quality Electronic Design*, pp. 108-113, 2008.
- [11] **D. Ganesan**, A. Mitev, J. Wang, Y. Cao, “Finite-point gate model for fast timing and power analysis,” *International Symposium on Quality Electronic Design*, pp. 657-662, 2008.
- [12] L. Cheng, Y. Lin, L. He, and Y. Cao, “Trace-based framework for concurrent development of process and FPGA architecture considering process variation and reliability,” *International Symposium on Field-Programmable Gate Arrays*, pp. 159-168, 2008.
- [13] **Y. Ye**, F. Liu, S. Nassif, Y. Cao, “Statistical modeling and simulation of threshold voltage variation under dopant fluctuations and line-edge roughness,” *9th Annual Austin CAS Conference*, 2008.
- [14] M. Agarwal, **V. Balakrishnan**, A. Bhuyan, K. Kim, M. Mizuno, B. C. Paul, **W. Wang**, Y. Cao, S. Mitra, “Optimized circuit failure prediction for aging: practicality and promise,” *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, 2008.
- [15] **A. Subramaniam, R. Singal, C.-C. Wang**, Y. Cao, “Design rule optimization of regular layout for leakage reduction in nanoscale design,” *Asia and South Pacific Design Automation Conference*, pp. 474-479, 2008. [acceptance rate: 35%]
- [16] **W. Zhao**, X. Li, M. Nowak, and Y. Cao, “Predictive technology modeling for 32nm low power design,” *International Semiconductor Device Research Symposium*, TA4-03, 2007.
- [17] **W. Wang**, Z. Wei, S. Yang, Y. Cao, “An efficient method to identify critical gates under circuit aging,” *International Conference on Computer Aided Design*, pp. 735-740, 2007.

- [18] **D. Ganesan**, D. Shanmugasundaram, A. Mitev, Y. Cao, J. Wang, "A robust finite-point based gate model considering process variations," *International Conference on Computer Aided Design*, pp. 692-697, 2007. [**acceptance rate: 27%**]
- [19] Y. Cao, C. C. McAndrew, "MOSFET modeling for 45nm and beyond," embedded tutorial, *International Conference on Computer Aided Design*, pp. 638-643, 2007. [**invited**]
- [20] **W. Wang**, V. Reddy, A. T. Krishnan, S. Krishnan, Y. Cao, "An integrated modeling paradigm of circuit reliability for 65nm CMOS technology," *Custom Integrated Circuits Conference*, pp. 511-514, 2007. [**acceptance rate: 33%**]
- [21] **W. Zhao**, F. Liu, K. Agarwal, D. Acharyya, S. Nassif, K. Nowka, Y. Cao, "Rigorous extraction of process variations for 65nm CMOS design," *European Solid-State Circuits Conference*, pp. 89-92, 2007.
- [22] **W. Wang**, V. Reddy, A. T. Krishnan, S. Krishnan, Y. Cao, "An integrated modeling paradigm of circuit reliability for 65nm CMOS technology," *SRC TECHNON*, 2007.
- [23] **A. Balijepalli**, **S. Sinha**, Y. Cao, "Compact modeling of carbon nanotube transistor for early stage process-design exploration," *International Symposium on Low Power Electronics and Design*, pp. 2-7, 2007. [**best paper award**]
- [24] **W. Wang**, S. Yang, S. Bhardwaj, **R. Vattikonda**, F. Liu, S. Vrudhula, Y. Cao, "The impact of NBTI on the performance of combinational and sequential circuits," *Design Automation Conference*, pp. 364-369, 2007. [**acceptance rate: 23%**]
- [25] **R. Singal**, **A. Balijepalli**, **A. Subramaniam**, F. Liu, S. Nassif, Y. Cao, "Modeling and analysis of non-rectangular gate for post-lithography circuit simulation," *Design Automation Conference*, pp. 823-828, 2007. [**acceptance rate: 23%**]
- [26] **M. Chen**, **W. Zhao**, F. Liu, Y. Cao, "Fast statistical circuit analysis with finite-point based transistor model," *Design, Automation and Test in Europe*, pp. 1391-1396, 2007.
- [27] **A. Balijepalli**, J. Ervin, Y. Cao, and T. Thornton, "Compact modeling of a PD SOI MESFET for wide-temperature designs," *International Symposium on Quality Electronic Design*, pp. 133-138, 2007.
- [28] **R. Vattikonda**, Y. Luo, A. Gyure, X. Qi, S. Lo, M. Shahram, Y. Cao, K. Singhal, and D. Toffolon, "A new simulation method for NBTI analysis in SPICE environment," *International Symposium on Quality Electronic Design*, pp. 41-46, 2007.
- [29] **T. Sairam**, **W. Zhao**, Y. Cao, "Optimizing FinFET technology for high-speed and low-power design," *Great Lakes Symposium on VLSI*, pp. 73-77, 2007. [**best paper award nominee**]
- [30] **W. Zhao**, F. Liu, K. Agarwal, D. Acharyya, S. Nassif, K. Nowka, Y. Cao, "Extraction and modeling of process variations for robust nanoscale design," *8th Annual Austin CAS Conference*, 2008.
- [31] B. T. Cline, K. Chopra, D. Blaauw, and Y. Cao "Analysis and modeling of CD variation for statistical static timing," *International Conference on Computer Aided Design*, pp. 60-66, 2006. [**acceptance rate: 24%**]
- [32] Y. Cao, **W. Zhao**, "Predictive technology model for nano-CMOS design exploration," *International Conference on Nano-Networks*, 2006. [**invited**]
- [33] S. Bhardwaj, **W. Wang**, **R. Vattikonda**, Y. Cao, S. Vrudhula, "Predictive modeling of the NBTI effect for reliable design," *Custom Integrated Circuits Conference*, pp. 189-192, 2006. [**acceptance rate: 33%**]

- [34] **R. Vattikonda, W. Wang, Y. Cao**, “Modeling and minimization of PMOS NBTI effect for robust nanometer design,” *Design Automation Conference*, pp. 1047-1052, 2006. **[acceptance rate: 24%]**
- [35] S. Bhardwaj, S. Vrudhula, Praveen Ghanta, Y. Cao, “Modeling of intra-die process variations for accurate analysis and optimization of nanoscale circuits,” *Design Automation Conference*, pp. 791-796, 2006. **[acceptance rate: 24%]**
- [36] **A. Balijepalli, J. Ervin, P. Joshi, J. Yang, Y. Cao, and T. J. Thornton**, “High-voltage CMOS compatible SOI MESFET characterization and SPICE model extraction,” *IEEE International Microwave Symposium*, pp. 1335-1338, 2006.
- [37] S. Bhardwaj, S. Vrudhula, and Y. Cao, “LOTUS: leakage optimization under timing uncertainty for standard-cell designs,” *International Symposium on Quality electronic Design*, pp. 717-722, 2006.
- [38] **W. Zhao and Y. Cao**, “New generation of predictive technology model for sub-45nm design exploration,” *International Symposium on Quality Electronic Design*, pp. 585-590, 2006. **[best paper award nominee; cited by 119]**
- [39] **M. Chen and Y. Cao**, “Analysis of pulse signaling for low-power on-chip global bus design,” *International Symposium on Quality electronic Design*, pp. 401-406, 2006.
- [40] S. Bhardwaj, Y. Cao, and S. Vrudhula, “Statistical leakage minimization using gate sizing, gate length biasing and threshold voltage selection,” *Asia and South Pacific Design Automation Conference*, pp. 953-958, 2006. **[best paper award nominee]**
- [41] J. Chen, L. T. Clark, Y. Cao, “Robust subthreshold design of high fan-in/out circuits,” *International Conference on Computer Design*, pp. 405-410, 2005.
- [42] Y. Cao and L. T. Clark, “Mapping statistical process variations toward circuit performance variability: an analytical modeling approach,” *Design Automation Conference*, pp. 658-663, 2005.
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Grants and Contracts

- Qualcomm, “Benchmarking Nanoscale Circuit Design with Predictive Technology Model,” 04/01/08 – 03/31/09, \$75,000
- National Science Foundation, “Self-Assembled Inductors: A New Paradigm in Nanoelectronics Design,” co-PI with Hongbin Yu, Bertan Bakkaloglu, Hao Yan, ASU, 09/01/07 – 08/31/10, \$650,000 [Share: 20% or \$130,000]
- Semiconductor Research Corporation, “Predictive Modeling and Simulation of Reliability Degradation in Nanoscale Circuits,” 07/01/07 – 06/31/10, \$150,000
- Qualcomm, “Benchmarking Nanoscale Circuit Design with Predictive Technology Model,” 06/08/07 – 03/31/08, \$75,000
- Focus Center Research Program (FCRP), the Gigascale System Research Center (led by University of California, at Berkeley), “System Performance Prediction for Reliable Nanoscale Integration,” 09/01/06 – 8/31/09, \$280,000
- Focus Center Research Program (FCRP), the Materials, Structures, and Devices Center (led by Massachusetts Institute of Technology) and the Center of Circuits and System Solutions (led by Carnegie Mellon University), “Predictive Technology Modeling for End-of-the-Roadmap and Post-Silicon Technologies,” 09/01/06 – 8/31/09, \$390,000
- National Science Foundation, “CAREER: Bridging the Technology-EDA Gap through Strategic Tools for Robust Nanometer Design,” 08/15/06 – 07/31/11, \$404,015
- Semiconductor Research Corporation, “Benchmarking Nanoscale Circuit Reliability with Predictive Technology Models,” 09/01/05 – 12/31/06, \$80,000
- Connection One, a National Science Foundation’s Industry/University Cooperative Research Center, “Ultra Low-Power Digital Logic Design for Nanometer Technology,” 07/01/06 – 09/30/06, \$40,000 [ASU internal competition]
- Microelectronics Advanced Research Corporation (MARCO), the Materials, Structures, and Devices Center (led by Massachusetts Institute of Technology) and the Center of Circuits and System Solutions (led by Carnegie Mellon University), “Predictive Technology Modeling for Robust Nanometer Design,” 04/16/05 – 12/31/06, \$174,700
- Semiconductor Research Corporation, “Robust Low Power Circuit Design with Predictive Technology Models,” co-PI with Lawrence Clark, ASU, 01/01-05 – 01/31/06, \$75,000 [Share: 40% or \$30,000]

Gifts from Industry

- IBM Corporation, Faculty Award for research on nanoelectronic design, \$25,000, 2007.
- IBM Corporation, Faculty Award for research on reliable system design, \$25,000, 2006.
- Intel Corporation, gift to support research on variation modeling and analysis, \$30,000, 2006.