Statement of Research, Teaching and Service

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I am currently a fourth-year Assistant Professor in the Department of Electrical Engineering at Arizona State University. I completed my Ph.D. from the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley in December 2002. After that, I worked as a post-doctoral researcher at the Berkeley Wireless Research Center. I joined ASU in November 2004. Since then, it has been an inspiring period of my academic career to experience and develop an integrated program of research, teaching, and professional service. Currently, I am supervising six Ph.D. graduate students and two Master graduate students working is the area of Nanoscale Integration and Modeling (the NIMO research group, available at http://www.eas.asu.edu/~nimo). So far, one Ph.D. student and four Master students have graduated from my research group, joining leading semiconductor companies.

In the following sections, I will provide details of my current and future research directions, teaching philosophy, and the synergies between these efforts. I will also summarize my contributions to both teaching and university service.

Current and Future Research

My areas of research are in the physical modeling and design of integrated circuits with nanoscale technologies, with the overarching goal to advance the state of the art in reliable design with nanoscale and biological devices. Physical device models are the essential interface between the underlying technology and integrated system design. Coupled with design automation tools, they significantly improve design productivity, providing key insights into process choices and design decisions. As the minute feature size rapidly scales into the 10nm regime, these demands are tremendously challenged. Examples of the challenges include the introduction of alternative materials and structures to traditional silicon transistors, the revolutionary transition toward post-silicon devices, and unavoidable amounts of process variations and reliability degradation. Driven by the increasingly complex and diverse nature of technological evolution, my research objective is to develop physical models and fundamental design solutions that can successfully respond to these challenges and enable early stage exploration.

Conducting early design exploration requires Predictive Technology Models (PTM) for future technology generations. At ASU, I currently lead the development of Predictive Technology Models for extremely scaled silicon devices toward the 10nm regime and beyond. PTM makes a far-reaching impact on early stage design research, allowing a designer to identify emergent challenges and explore solutions up front. PTM is the *de facto* predictive transistor models for both academic and industrial researchers. Since the web release of PTM (http://www.eas.asu.edu/~ptm), more than 1500 papers have been published by independent research teams all over the world using PTM models. PTM is also adopted by advanced analog and digital design courses in many universities, as well as leading industry practice.

Beyond the 10nm technology generation, more radical solutions will be vital to meet the scaling criteria. There are several revolutionary technologies such as carbon nano-tubes and molecular devices that promise to be alternative technology choices. In particular, carbon nano-tube field effect transistors (CNT-FETs) are very attractive for future integrated circuit applications. While there have been significant accomplishments in scientific discovery, it is just the beginning of the engineering research that is required to transfer the science into device, circuit, and system explorations. In this context, I recently outreached PTM to the compact modeling of CNT-FETs and other emerging devices. Our modeling of CNT-FETs received the Best Paper Award at 2007 International Symposium on Low-Power Electronics and Design. At the dawn of the post-silicon age, PTM provides a broad understanding of the underlying physics, helping shed light on the enormous design potential.

In addition, I have worked on the key limiting factors for future integrated system design: variability and reliability. To maintain design predictability with nanoscale devices, I am driving the modeling paradigm shift from the traditional corner-based approach to a suite of statistical modeling solutions, including extraction methods, the decoupling of variation sources, and highly efficient simulation strategies. The key modeling challenge under variations is to identify systematic variation components, develop predictive models for performance analysis, and incorporate them into statistical design tools. These solutions will allow a designer to build reliable circuits and systems to meet multi-dimensional performance requirements with a guaranteed level of confidence.

My work in the areas above was awarded by the NSF Faculty Early Career Development program (CAREER) in 2006. Presently I am the PI of the NSF CAREER project, two Focus Center Research Program (FCRP) projects, one Semiconductor Research Corporation (SRC) project, one industrial project, as well as a co-PI of one NSF project through the collaboration with faculties across the Fulton School of Engineering and the Biodesign Institute at ASU. In addition, I work with many semiconductor companies to transfer the newly developed solutions into their tools, such as Intel, IBM, Texas Instruments, Qualcomm, and Synopsys. Research grants that I have received since 2005 total $1,828,715. Since I joined ASU, I have published 16 journal papers, 43 conference papers, 8 invited talks, and two patent applications. Many of my research results were compiled into a book that I co-authored, entitled *Nano-CMOS Circuit and Physical Design*, published by John Wiley & Sons, Inc. This text is a useful reference for practicing engineers but also serve as an up-to-date textbook for graduate level semiconductor device and circuit design courses.

For future research, I plan to continue my work in the area of the physical modeling and reliable integration of extremely scaled silicon device, nanotechnology, and biological devices. As technology scaling approaches the ultimate limits that are defined by physics and the fabrication process, the design field will expand to include both end-of-the-roadmap silicon and post-silicon devices into nanoscale systems in the 10nm regime. One application that I am particularly interested in is heterogeneous integration based on the technique of self-assembled DNA scaffolds. Although post-silicon devices have demonstrated faster switching, lower power consumption and better scalability, tremendous research questions still remain in materials, alignments, and yield. The hybrid integration of both nanoscale silicon device and emerging technologies will offer an optimal solution in the spectrum of manufacturability, reliability, and performance. This hybrid scheme will not only provide the advantages in system performance; its potential compatibility with current silicon design infrastructure further maximizes the economic benefit for the semiconductor industry.

In summary, by developing physical models and interdisciplinary solutions, my research aims to ensure a timely and smooth transition from silicon-based design to robust integration with post-silicon technologies. I am excited in pursuing further research in these areas and look forward to collaborating with other faculties and students who share the same interests.

Teaching

The principal goal of my teaching effort is to introduce students to the role of nanoscale technology advances in integrated system design both early and often, and prepare a diverse population of students for academia and industry with relevant design knowledge.

Driven by the rapid scaling of semiconductor technology, the design of integrated circuits requires a broad and interdisciplinary knowledge of manufacturing, physical modeling, circuit design, and design automation tools. It also requires a much deeper understanding of statistical design principles as process variations become pronounced. Currently these topics are not addressed adequately in university curricula.

The lack of dedicated higher-education courses consequently creates a growing knowledge gap between the underlying technology and state-of-the-art design practice.

To bridge this gap, I believe that the most effective approach is to introduce key technology concepts and modeling topics in a circuit design course. Therefore, at ASU, I revised the curricula of two undergraduate digital design courses (EEE 333 "HDL and programmable logic" and EEE 425 "Digital systems and circuits") and a graduate VLSI design course (EEE 525 "VLSI design") through the emphasis on the fundamental understanding of silicon technology and an introduction of process and design uncertainties in circuit analysis. The goal is to deliberately transfer a comprehensive view to future design engineers earlier in the education process. This practice is reinforced by lab experiments and design projects with well defined objectives.

In addition to the regular courses, I developed a new graduate course on modeling and analysis for nanoscale circuit design (EEE 598). The concept of technology-design integration is central to the course. This new course presented significant technological issues in advanced integrated circuit design, including power consumption, process variations, signal integrity, reliability degradation, and others. My recently published book, entitled *Nano-CMOS Circuit and Physical Design*, provides a timely attention to these topics and serves as an up-to-date textbook, along with well selected papers for supplemental information. This course is driven by innovative design projects that serve as a test base for graduate students to understand the basic concepts and initialize significant work in this area. To prepare a strong and novel curriculum, I particularly encourage often and interactive feedbacks to assess the new course.

As future nanoscale design becomes larger and more complex, I am continuously interested in teaching the fundamental theories behind advanced electron devices, as well as contemporary design methodologies of integrated systems. Given the opportunity to share my learning with students, I plan to motivate my students to expand their boundaries, stay current with advances outside their immediate discipline, and build broad and unique viewpoints. With the concept of a teacher as a guide along with the goal of encouraging students to achieve, I seek to not only reveal the essence of the subject matter, but also to inspire students along the road of exploration.

Professional Service

I recognize the importance of university, professional, and community service. Along this direction, I have emphasized involvement in program committees and chairing of technical conferences, with the expectation to develop increasing visibility and responsibility. I co-founded the IEEE/ACM Workshop on Compact Variability Modeling, 2008. Currently I am serving as the chair/co-chair of subcommittees in IEEE International Conference on Computer-Aided Design, IEEE International Reliability Physics Symposium, and IEEE/ACM International Symposium on Low Power Electronics Design. I have been on the technical program committee of many circuit design and design automation conferences, such as Design Automation Conference, International Conference on Computer-Aided Design, and International Symposium on Low-Power Electronics and Design. I am also a member of the IEEE Electron Device Society Compact Modeling Technical Committee.

As a Master graduate advisor, I provide constant advice to help the students develop appropriate programs of study. In parallel with the continuous development of professional services, I anticipate taking more responsibility for departmental and institutional needs.

My last three years in the Department of Electrical Engineering have been exciting, energizing and productive. In the coming years, I strongly believe that my current and future teaching and research efforts will increase the significance and visibility of the Department of Electrical Engineering, the Fulton School of Engineering and Arizona State University. I look forward to continuing my career development here towards an internationally recognized interdisciplinary program.